



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,123	10/30/2003	S. Jay Chey	YOR920030511US1	4971
23334	7590	10/04/2004	EXAMINER	
FLEIT, KAIN, GIBBONS, GUTMAN, BONGINI & BIANCO P.L. ONE BOCA COMMERCE CENTER 551 NORTHWEST 77TH STREET, SUITE 111 BOCA RATON, FL 33487			DOUGHERTY, ANTHONY T	
			ART UNIT	PAPER NUMBER
			2863	
DATE MAILED: 10/04/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/699,123

Applicant(s)

CHEY ET AL.

Examiner

Anthony T. Dougherty

Art Unit

2863

RW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☒ Claim(s) 21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 21 objected to because of the following informalities: The last line of claim 21 recites “adjacent to insulating-insulating layer” it is assumed by the examiner that this is a typographical and for prior art examination purposes has been treated as if it read “adjacent to electrical-insulating layer”.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-21 rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,787,870 to Wienand et al.

With regard to claims 1, 16, and 21 Wienand et al. discloses a system for measuring thermal distribution of an electronic device during operation (see abstract) with a heat sink in thermal communication with the electronic device (see column 4 line 17-29), an electrical-insulating layer between the electronic device and the heat sink (see column 4 line 20-23 & Figure 1a), a plurality of thermal sensors located adjacent to the electrical-insulating layer (see

Art Unit: 2863

column 3 line 62 through column 4 line 3), and the thermal sensor is located within one or more thin film circuit layers disposed on the electrical-insulating layer (see column 3 line 62 through column 4 line 3 & column 2 line 25 through line 30).

With regard to claims 2 and 17, and applying the rejection of claims 1 and 16 above, Wienand et al. discloses a module for receiving information from the thermal sensors during operation of the electronic device when the device is operating under a range of operating conditions specified for the electronic device (see column 4 line 24-29).

With regard to claims 3 and 18, and applying the rejection of claims 2 and 17 above, Wienand et al. discloses a processor coupled to the module for generating a thermal distribution of the electronic device based on the thermal information received from the thermal sensors (see column 4 line 24-29).

With regard to claims 4 and 19, and applying the rejection of claims 3 and 18 above, Wienand et al. discloses the thermal sensor is a thin film thermocouple or thin film resistor (see column 3 line 66 through column 4 line 3).

With regard to claim 5, and applying the rejection of claim 4 above, Wienand et al. discloses the thermal sensors comprise at least twenty five thin film thermocouples (see column 2 line 39-44).

With regard to claim 6, and applying the rejection of claim 4 above, Wienand et al. discloses each of the sensors has a junction area of about 10,000 microns<sup>2</sup> (see column 2 line 25-30).

With regard to claim 7, and applying the rejection of claim 3 above, Wienand et al. discloses the heat sink is any one of a copper element and a silicon element (see column 1 line 34-35).

With regard to claim 8, and applying the rejection of claim 3 above, Wienand et al. discloses each of the sensors is a thin film resistor (see column 3 line 66 through column 4 line 3).

With regard to claim 9, and applying the rejection of claim 8 above, Wienand et al. discloses at least twenty five thin film resistors (see column 2 line 39-44).

With regard to claim 10, and applying the rejection of claim 8 above, Wienand et al. discloses each of the sensors has a junction area of about 10,000 microns<sup>2</sup> (see column 2 line 25-30).

With regard to claim 11, and applying the rejection of claim 8 above, Wienand et al. discloses the heat sink is any one of a copper element and silicon element (see column 1 line 34-35).

With regard to claim 12, and applying the rejection of claim 3 above, Wienand et al. discloses the electrical-insulating layer comprises a thin film of at least one of silicon nitride, silicon dioxide and alumina (see column 4 line 11-12).

With regard to claim 13, and applying the rejection of claim 12 above, Wienand et al. discloses the electrical-insulating layer has a thickness of less than 1 micron (see column 3 line 5-11).

With regard to claims 14 and 20, and applying the rejection of claims 3 and 18 above, Wienand et al. discloses the sensors comprise patterned films having a thickness from about 10 nm to about 5 microns (see column 2 line 39-44).

With regard to claim 15, and applying the rejection of claim 4 above, Wienand et al. discloses the thermal impedance is governed by the heat sink (see column 3 line 53-61).

### ***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,631,638 to James et al. because it teaches measuring a heat distribution of an electronic device located on a substrate using a plurality of thermal sensors on the substrate but separate from the electronic device and without a heat sink.

International Application Publication No. WO 03/046702 A2 to Meir because it teaches controlling the temperature of an electronic device using a sensor attached to a thermocouple between the electronic device and a heat sink.

U.S. Patent No. 5,825,625 to Esterberg et al. because it teaches using a heat sink with an electronic device for transferring heat.

U.S. Patent No. 6,058,012 to Cooper et al. because it teaches using a single temperature sensor between an electronic device and a heat sink to measure the temperature of the electronic device.

U.S. Patent No. 6,496,118 to Smith because it teaches using solid conductive positive temperature coefficient of resistance (PCTR) polymeric tape between an electronic device and a heat sink for measuring an over temperature condition of the electronic device.

U.S. Patent No. 6,515,285 to Marshall et al. because it teaches using radiation to measure ambient temperature variations near a heat sink attached to an electronic device.

U.S. Patent No. 6,092,926 to Still et al. because it teaches monitoring the operating temperature of an electronic device with a heat sink attached using a sensor between a printed circuit board and a thermal pad attached to the electronic device.

U.S. Patent No. 6,020,820 to Chiang because it teaches measuring the temperature of an electronic device using a heat sensor between the electronic device and a heat sink.

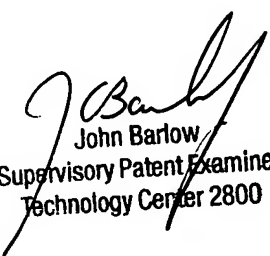
Art Unit: 2863

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T. Dougherty whose telephone number is (571) 272-2273. The examiner can normally be reached on Monday through Friday from 8 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
atd

  
John Barlow  
Supervisory Patent Examiner  
Technology Center 2800